2023 International VLSI

Symposium on Technology, Systems and Applications

April 17-20, 2023 Hsinchu, Taiwan

Call for Papers

Highlights

The 2023 International VLSI Symposium on Technology, Systems and Applications will be held on April 17-20, 2023 at the Ambassador Hotel, Hsinchu, Taiwan. The symposium has been kicked-off since 1983. It is a premiere conference in Taiwan and received up to 1,000 participants every year. It provides a unique opportunity to network with VLSI leading experts worldwide. Original and unpublished papers on all aspects of advanced VLSI technology and applications are solicited.

The 4-day event will include: 3 Plenary Sessions, 2 Joint Special Sessions, 3 Tutorials, 2 Industrial Sessions, Special Sessions (invited), and Paper Sessions.

Hsinchu City: The well-known Taiwan's Silicon Valley is based with clusters of world-class high Tech. IC manufacturing and design. It is one-hour driving distance from Taipei, 40 minutes from the airport. Industry attendees may take this opportunity to visit Science Park business unit and academia attendees may visit major universities/institutes of Taiwan, either in Hsinchu, or down to the south by the high speed train within one hour.

Paper Submission

Prospective authors are invited to submit papers starting in August through the symposium website at https://expo.itri.org.tw/ 2023VLSI TSADAT. Presentation at the Symposium is in English. For an accepted paper to be published in the proceedings, one of its co-author(s) MUST register and attend the symposium to present the paper. Note that each accepted paper shall be accompanied by a distinct registration; that is, two registrations are required for presenting two papers even if the presenter is the same. All papers presented at the symposium will be published in the proceedings as submitted without revisions. Authors of accepted papers must transfer copyright to IEEE by utilizing the electronic IEEE Copyright Form (eCF) for inclusion in the IEEE Xplore database. No-show papers will not be submitted to the IEEE Xplore database.

Further detailed instructions on papers submission to TSA and DAT domains, please refer to the following pages of Call For Papers or visit the "Authors" section of the website.

Submission to TSA (Technology, Systems and Applications):
https://expo.itri.org.tw/2023TSA/Submission

Submission to DAT (Design, Automation and Test):
https://expo.itri.org.tw/2023DAT/Submission

Scope

To address the needs of ever-changing semiconductor industry and the tight coupling between technology and design, VLSI-TSA and VLSI-DAT Symposia will be merged into one Symposium in 2023. Original and unpublished papers on all aspects of advanced VLSI technology, systems, applications, design, automation, and test are solicited.

Further details on the paper scope of TSA and DAT domains, please refer to the following pages of Call For Papers or visit the "Authors" section of the website.

Submission to TSA (Technology, Systems and Applications):
https://expo.itri.org.tw/2023TSA/Submission

Submission to DAT (Design, Automation and Test):
https://expo.itri.org.tw/2023DAT/Submission

Further Information

Additional information, including TSA Student Paper Award, DAT Best Paper Award, and Financial support for students, please visit the Symposium website at: **https://expo.itri.org.tw/2023VLSITSADAT/**

COVID-19 Watch: 2023 International VLSI Symposium on Technology, Systems and Applications is planned for an in-person/on-site event. In the meantime, we will keep Hybrid meeting (same as 2022) if COVID-19 still keeps a threat to the convention, i.e., arranging overseas presenters to provide a pre-recorded video for presentation on condition that they render into travel restrictions.

General Chair
Shih-Chieh Chang
Industrial Technology Research Institute

TSA Symposium Chair
Peide Ye
Purdue University

DAT Symposium Chairs
Atsushi Takahashi
Tokyo Institute of Technology

Chih-Tsun Huang
National Tsing Hua University

TSA Program Chairs
Jenn-Gwo Hwu
National Taiwan University

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ITRI
Industrial Technology
Research Institute

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SCOPE

- Front-end CMOS and foundry technology
- Standalone memory: DRAM, FLASH, emerging memory technology
- Ultra-low power CMOS and embedded memory
- Advanced process modules: e.g. gate stack, junction, strain/channel engineering, low-R contact, low-C spacer/ILD, interconnect technology, ALE and selective deposition, etc.
- Nano-patterning: multiple patterning, directed self-assembly, EUV, etc.
- Advanced CMOS process and devices: Ge, SiGe, III-V, FinFET, GAAFET, low-dimensional materials and devices, 2D and nanowire devices
- BEOL compatible devices for 3D integration
- Material, process and device modeling

- Reliability physics, characterization and measurements
- Advanced packaging and 2.5D/3D integration
- TFT and organic electronics
- MEMS, imagers and sensors
- Power and analog IC devices and technology
- Photonics and beyond CMOS technology
- RF & THz process, device and integration technology
- Energy harvesting technology
- Wearable and IoE enabling technologies
- Quantum phenomena and information technologies
- Neuromorphic devices and materials for brain-inspired computing
- Device/circuit technologies for AI deep learning applications
- Advanced manufacturing technology, metrology and yield

PAPER SUBMISSION GUIDELINES

Camera-ready manuscript (**2 pages** including figures and tables) should be submitted electronically in PDF format through the symposium website at https://expo.itri.org.tw/2023TSA/Submission. Accepted papers MUST be presented by one of the authors at the conference to warrant the paper publication in the conference proceedings. The presentation is in English and will be limited to 15 minutes with an additional 5 minutes for discussion. All paper presenters are required to register for the symposium. All papers presented at the symposium will be published in the proceedings as submitted without revisions. Authors of accepted papers must transfer copyright to IEEE by utilizing the electronic IEEE Copyright Form (eCF) for inclusion in the IEEE Xplore database. No-show papers will not be submitted to the IEEE Xplore database.

STUDENT SUBSIDY

Student Travel financial support for attending 2023 International VLSI Symposium on Technology Systems and Applications is available for full-time student presenters living outside of Taiwan, and up to 65% discount for all students in registration fee.

BEST STUDENT PAPER AWARD

The selection will be based on the paper quality evaluated by technical committee members, as well as the presentation of the paper at the symposium. The paper should be presented by the key author who is a full-time student at the time of paper presentation. The Best Student Paper Award will be presented to the winning student at the next year's symposium.

LATE NEWS PAPERS

A very limited number of high quality Late News Papers will be accepted. Note that Late News Papers are not eligible for the best student paper award.

IMPORTANT DATES (**Note:** All are based on Taiwan time, which is eight hours ahead of Greenwich Mean Time (GMT+8).)

Paper Submission Deadline	Nov. 1, 2022
Notification of Acceptance	Dec. 30, 2022
Late News Paper Submission Deadline	Jan. 15, 2023
Author Registration Deadline	Feb. 28, 2023

TSA Program Chairs

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TSA Secretariat

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The 2023 International VLSI Symposium on Technology, Systems and Applications will be held on April 17-20, 2023, at the Ambassador Hotel, Hsinchu, Taiwan. Original and unpublished papers on all aspects are solicited, including but not limited to the following scope:

Analog, Mixed-Signal, and RF Design
- RF, Analog and Mixed-Signal Circuits
- Energy-Harvesting and Power Management Circuits
- Biomedical Circuits
- Sensor and Interface Circuits
- Wired and IO Design

Digital, Memory, and AI Chip Design
- Communication Baseband Designs
- Computing-in-Memory
- Digital Circuits and ASICs
- Hardware Security and Trust
- Low Voltage & Ultra Low-Power Circuits and Systems
- Memory Circuits and Systems
- Memristive and Neuromorphic Circuits
- Security Circuits for IoT and AI
- Specialized Hardware

Application, System, Software and Hardware Architecture
- AI for Systems and Systems for AI
- CPU, DSP, and Multicore Architectures
- Domain-Specific Architectures and Accelerators
- Embedded System and Software
- Hardware-efficient AI Methods
- Multimedia Processing Designs
- SoC (System on Chip) and NoC (Network on Chip) Architectures
- Software/Hardware Co-Design and System Compiler
- SiP (System-in-Package) and Heterogeneous Integration Designs

Design Automation and Test Methodology
- AI for Design Automation & Test
- Behavioral, Logic, and Physical Synthesis
- Design Automation & Test for Analog/Mixed-Signal/RF, 2D/3D IC, Memory, Biochip, AI Chips, and Emerging Systems
- Design for Manufacturability, Testability, and BIST
- Design Verification, Modeling, and Simulation
- Power/Thermal/Timing Optimization and On-Chip Monitoring
- Silicon Debug, Diagnosis, ECO, and Yield/Reliability Enhancement
- Test Generation, Compression, and Test Standards

Emerging Technology
- Circuit & IP Design Based on New Transistor Technology, e.g., Fork-Fin FET, Sheet FET, GAA FET, and C-FET
- Cryogenic Circuits and Systems
- Flexible and Printable Electronics
- Medical/Bio-electronics/Bio-inspired Chip Designs
- Quantum Computing
- Silicon Photonics

GENERAL INSTRUCTIONS
- Prospective authors are asked to submit their work in **two stages**.
  - ※ In **Stage One** (abstract submission), a title, an 80- to 100-word abstract, and a list of all co-authors must be submitted via the conference submission page (https://expo.itri.org.tw/2023DAT/Submission) before **October 15, 2022**. No abstract submissions after the deadline.
  - ※ In **Stage Two** (paper submission), authors must electronically submit the self-contained paper with figures and tables via the same submission page before **November 01, 2022**.
- The submitted manuscript must be 2 or 4 pages, double-columned, IEEE-style compatible, in PDF format only. Any submissions not adhering to the rules will be rejected immediately without review.
- It adopts the **double-blind** review process. Please DO NOT reveal your name(s) or affiliation(s) anywhere in the submitted manuscript for the first paper submission.
- Before submitting your abstract/paper, please review the information on IEEE Intellectual Property Rights at https://www.ieee.org/publications/rights/index.html
- The notices of acceptance will be sent out to authors on December 30, 2022.
- Any changes on the title and author list or withdrawal after acceptance must be approved by DAT symposium Program Chairs.
- For an accepted paper to be published in the proceedings, one of its co-author(s) MUST register and attend the symposium to present the paper. Note that each accepted paper shall be accompanied by a distinct registration; that is, two registrations are required for presenting two papers even if the presenter is the same.
- Presentation of accepted papers at the symposium must be in English. The final manuscripts of all accepted papers will be published as submitted in the proceedings.
- No-show papers will not be included in the symposium proceedings and will not be submitted to the IEEE Xplore database.
- Please refer to the detailed information on the conference website for authors: https://expo.itri.org.tw/2023VLSITSADAT

STUDENT SUBSIDY
Financial supports are available for full-time student presenters living outside of Taiwan.

BEST PAPER AWARD
Three best papers will be selected this year through a rigorous evaluation process conducted by the program committee and session chairs.

IMPORTANT DATES Note: all are based on Taiwan time (GMT+8).

Deadline for Title/Abstract Submission	**October 15, 2022**
Deadline for Camera-Ready Paper Submission	**November 01, 2022**
Notification of Acceptance	December 30, 2022
Deadline for Final Paper (IEEE compatible version) Submission	January 31, 2023
Deadline for Author Registration Deadline	February 28, 2023

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